# PATENT COOPERATION TREATY

# PCT

## INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

| Applicant's or agent's file reference<br>20302314/SJ | **FOR FURTHER ACTION** | See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416). |
|---|---|---|
| International Application No.<br>**PCT/SG2003/000223** | International Filing Date *(day/month/year)*<br>19 September 2003 | Priority Date *(day/month/year)*<br>19 September 2003 |

International Patent Classification (IPC) or national classification and IPC

**Int. Cl.** [7] H01L 21/4763, 21/285, 23/36, 23/367, 23/373, 31/024, 31/052, 31/18, H01S 5/024

Applicant

TINGGI TECHNOLOGIES PRIVATE LIMITED et al

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 3 sheets, including this cover sheet.

   [X] This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of **11** sheet(s).

3. This report contains indications relating to the following items:

   - I [X] Basis of the report
   - II [ ] Priority
   - III [ ] Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV [ ] Lack of unity of invention
   - V [X] Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI [ ] Certain documents cited
   - VII [ ] Certain defects in the international application
   - VIII [ ] Certain observations on the international application

| Date of submission of the demand<br>13 April 2005 | Date of completion of the report<br>5 October 2005 |
|---|---|
| Name and mailing address of the IPEA/AU<br>AUSTRALIAN PATENT OFFICE<br>PO BOX 200, WODEN ACT 2606, AUSTRALIA<br>E-mail address: pct@ipaustralia.gov.au<br>Facsimile No. (02) 6285 3929 | Authorized Officer<br>**MICHAEL HALL**<br>Telephone No. (02) 6283 2474 |

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
**PCT/SG2003/000223**

## I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed.

☒ the description, pages **1-2, 8-11,** as originally filed,
pages , filed with the demand,
pages **3-7,** received on **29 September 2005** with the letter of **21 September 2005**

☒ the claims, pages , as originally filed,
pages , as amended (together with any statement) under Article 19,
pages , filed with the demand,
pages **12-17,** received on **29 September 2005** with the letter of **21 September 2005**

☒ the drawings, pages **1-5,** as originally filed,
pages , filed with the demand,
pages , received on with the letter of

☐ the sequence listing part of the description:
pages , as originally filed
pages , filed with the demand
pages , received on with the letter of

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages

☐ the claims, Nos.

☐ the drawings, sheets/fig.

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report*

**V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

| | | | |
|---|---|---|---|
| Novelty (N) | Claims | **1-52** | **YES** |
| | Claims | | **NO** |
| Inventive step (IS) | Claims | **1-52** | **YES** |
| | Claims | | **NO** |
| Industrial applicability (IA) | Claims | **1-52** | **YES** |
| | Claims | | **NO** |

2. Citations and explanations (Rule 70.7)

Citation

D1 : US 6562648 B1

NOVELTY (N) and INVENTIVE STEP (IS)

D1 represents the closest prior art, and teaches, referring to either of Figures 2b or 3b thereof, a semiconductor laser diode device comprising InGaN epitaxial layers 1110, first ohmic contact 1118, a thermally-conducting copper layer 1119 of thickness 100-500 microns applied by electroplating; and a second ohmic contact 1020 (see also column 4 line 54, column 5 lines 27-28, and column 7 lines 21-42 of D1).

No obvious combination of the prior art teaches or suggests electroplating a layer of conductive metal on a semiconductor device formed on a substrate and then removing the substrate, as per claims 1-28, 47-52; nor interposing an adhesive layer between a first ohmic contact and a thermally conductive layer as per claims 29-42; nor forming a first ohmic contact on GaN-related epitaxial layers of a semiconductor device formed on a substrate, removing the substrate, and forming a second ohmic contact as per claims 42-46. Hence the claims are considered to be novel and inventive.

INDUSTRIAL APPLICABILITY (IA) claims 1-52

The subject matter of the claims is applicable to the industrial manufacture of GaN semiconductor devices.

Known LED chips grown on sapphire substrates require two wire bonds on top of the chip. This is necessary because sapphire is an electrical insulator and current conduction through the 100-micron thickness is not possible. Since each wire bond pad takes about 10-15% of the wafer area, the second wire bond reduces the number of chips per wafer by about 10-15% as compared to single-wire bond LEDs grown on conducting substrates. Almost all non-GaN LEDs are grown on conducting substrates and use one wire bond. For packaging companies, two wire bonding reduces packaging yield, requires modification of one-wire bonding processes, reduces the useful area of the chip, and complicates the wire bonding process and thus lowers packaging yield.

Sapphire is not a good thermal conductor. For example, its thermal conductivity at 300K (room temperature) is 40W/Km. This is much smaller than copper's thermal conductivity of 380 W/Km. If the LED chip is bonded to its package at the sapphire interface, the heat generated in the active region of the device must flow through 3 to 4 microns of GaN and 100 microns of sapphire to reach the package/heat sink. As a consequence, the chip will run hot affecting both performance and reliability.

For GaN LEDs on sapphire, the active region where light is generated is about 3-4 micron from the sapphire substrate.

**Summary of the Invention**

In accordance with a preferred form of the present invention, there is provided a method for fabrication of a semiconductor device on a substrate, the semiconductor device having a plurality of layers; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the semiconductor device remote from the substrate and close to the device layer; and

(b) removing the substrate.

The semiconductor device may be a silicon-based device.

In accordance with another form, there is provided a method for fabrication of a light emitting device on a substrate, the light emitting device having a plurality of layers with an active layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the semiconductor device remote from the substrate and close to the active layer; and

PCT/SG2003/00223
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(b) removing the substrate.

For both forms, the thermally conductive layer may be as a heat sink, and may be of a thickness in the range of from 3 microns to 300 microns, preferably 50 to 200 microns.

In a further form, the present invention provides a method for fabrication of a semiconductor device on substrate, the semiconductor device having a plurality of layers; the method including the steps:

(a) applying a seed layer of a thermally conductive metal to a first surface of the semiconductor device remote from the substrate;

(b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer, the thermally conductive metal of sufficient thickness to provide a heat sink; and

(c) removing the substrate.

Prior to the seed layer being applied, the layers may be coated with an adhesion layer. Before the electroplating of the relatively thick layer the seed layer may be patterned with photoresist patterns; the relatively thick layer being electroplated between the photoresists.

The seed layer may be electroplated without patterning and with patterning being performed subsequently. Patterning may be by photoresist patterning and then wet etching. Alternatively, it may be by laser beam micro-machining of the relatively thick layer.

Between steps (b) and (c) there may be performed the additional step of annealing the layers to improve adhesion.

Preferably, the photoresists are of a height of at least 15 to 500 microns, more preferably 50 to 200 microns, and have a thickness in the range 3 to 500 microns. More preferably, the photoresists have a spacing in the range of 200 to 2,000 microns, preferably 300 microns.

The relatively thick layer may be of a height no greater that the photoresist height. Alternatively, the conductive metal layer may be electroplated to a height greater

than the photoresist and be subsequently thinned. Thinning may be by polishing or wet etching.

After step (c) there may be included an extra step of forming on a second surface of the semiconductor device remote from the relatively thick layer, a second ohmic contact layer. The contact layer may be a second ohmic contact layer. The second ohmic contact layer may be one of opaque, transparent, and semi-transparent, and may be either blank or patterned. Ohmic contact formation and subsequent process steps may be carried out. The subsequent process steps may include deposition of wire bond pads. The exposed second surface of the semiconductor device may be cleaned and etched before the second ohmic contact layer is deposited onto it. The second ohmic contact layer may not cover the whole area of the second surface of the semiconductor device.

The semiconductor devices may be tested on the layers, and the layers may be subsequently separated into individual devices.

The semiconductor devices may be fabricated without one or more of: lapping, polishing and dicing.

The semiconductor device comprises a plurality of epitaxial layers, a first ohmic contact layer being on a first surface of the epitaxial layers remote from the substrate. The first ohmic contact layers may be on p-type layers of the epitaxial layers; and the second ohmic contact layer may be formed on n-type layers of the expitaxial layers.

After step (c), dielectric films may be deposited on the epitaxial layers. Openings may then be cut in the dielectric and second ohmic contact layer and bond pads deposited on the epitaxial layers. Alternatively, after step (c), electroplating of a thermally conductive metal (or other material) on the epitaxial layers may be performed.

The invention is also directed to a semiconductor device fabricated by the above method. The invention, in a preferred aspect, also provides a light emitting diode or a laser diode fabricated by the above method.

In a further aspect, the present invention provides a semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the

epitaxial layers, a relatively thick layer of a thermally conductive metal on the first ohmic contact layer to form a heat sink, and a second ohmic contact layer on a second surface of the epitaxial layers; the relatively thick layer being applied by electroplating.

There may be an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer.

The relatively thick layer may be at least 50 micrometers thick; and the second ohmic contact layer may be a thin layer in the range of from 3 to 500 nanometers. The second ohmic contact layer may be transparent, semi-transparent or opaque; and may include bonding pads.

For all forms of the invention, the thermally conductive metal may be copper.

There may be a seed layer of the thermally conductive metal applied to the adhesive layer.

The semiconductor device may be one of: a light emitting diode, a laser diode, and a transistor device.

In yet another form, there is provided a semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer, and a seed layer of a thermally conductive metal on the adhesive layer.

There may be further included a relatively thick layer of the thermally conductive metal on the seed layer.

A second ohmic contact layer may be provided on a second surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers. The second ohmic contact layer may comprise bonding pads; and may be one of: opaque, transparent, and semi-transparent.

The thermally conductive metal may comprise copper; and the epitaxial layers may comprise GaN-related layers.

The semiconductor device may be a light emitting device.

In a penultimate form, the present invention provides a method of fabrication of a semiconductor device, the method including the steps:

(a) on a substrate with a plurality of epitaxial layers comprising multiple GaN-related epitaxial layers, forming a first ohmic contact layer on a first surface of the epitaxial layers;

(b) removing the substrate from the epitaxial layers; and

(c) forming a second ohmic contact layer on a second surface of the epitaxial layers, the second ohmic contact layer having bonding pads formed thereon.

The second ohmic contact layer may be for light emission; and may be opaque, transparent, or semi-transparent. The second ohmic contact layer may be blank or patterned.

In a final form, there is provided a semiconductor device fabricated by the above method.

The semiconductor device may be a light emitting diode or a laser diode.

**Brief Description of the Drawings**

In order that the invention may be better understood and readily put into practical effect there shall now be described by way of non-limitative example only a preferred embodiment of the present invention, the description being with reference to the accompanying illustrative (and not to scale) drawings in which:

Figure 1 is a schematic representation of a semiconductor device at a first stage in the fabrication process;

Figure 2 is a schematic representation of the semiconductor device of Figure 1 at a second stage in the fabrication process;

Figure 3 is a schematic representation of the semiconductor device of Figure 1 at a third stage in the fabrication process;

Figure 4 is a schematic representation of the semiconductor device of Figure 1 at a fourth stage in the fabrication process;

Figure 5 is a schematic representation of the semiconductor device of Figure 1 at a fifth stage in the fabrication process;

**The claims:**

1. A method for fabrication of a semiconductor device on substrate, the semiconductor device having a plurality of layers; the method including the steps:
   (a) applying a seed layer of a thermally conductive metal to a first surface of the semiconductor device;
   (b) electroplating a relatively thick layer of the thermally conductive metal on the seed layer, the thermally conductive metal of sufficient thickness to provide a heat sink; and
   (c) removing the substrate.

2. A method as claimed in claim 1, wherein the first surface is coated with an adhesion layer prior to application of the seed layer.

3. A method as claimed in claim 1 or claim 2, wherein the seed layer is patterned with photoresist patterns before the electroplating step (b).

4. A method as claimed in claim 3, wherein the electroplating of the relatively thick layer is between the photoresist patterns.

5. A method as claimed in any one of claims 1 to 4, wherein between steps (b) and (c) there is performed the additional step of annealing the layers to improve adhesion

6. A method as claimed in claim 3 or claim 4, wherein the photoresist patterns are of a height in the range 15 to 500 micrometers.

7. A method as claimed in claim 3 wherein the photoresist patterns have a thickness in the range 3 to 500 micrometers.

8. A method as claimed in any one of claims 3, 4, 6 and 7, wherein the photoresist patterns have a spacing in the range of 200 to 2,000 microns.

9. A method as claimed in any one of claims 1 to 8, wherein the seed layer is electroplated in step (b) without patterning, patterning being performed subsequently.

10. A method as claimed in claim 9, wherein patterning is by photoresist patterning and then wet etching.

11. A method as claimed in claim 9, wherein patterning is by laser beam micro-machining of the relatively thick layer.

12. A method as claimed in any one of claims 3 to 11, wherein the relatively thick layer is of a height no greater that the photoresist height.

13. A method as claimed in any one of claims 3 to 11, wherein the relatively thick layer of thermally conductive metal is electroplated to a height greater than the photoresist and is subsequently thinned.

14. A method as claimed in claim 13, wherein thinning is by polishing or wet etching.

15. A method as claimed in any one of claims 1 to 14, wherein after step (c) there is included an extra step of forming on a second surface of the semiconductor device a second ohmic contact layer, the second ohmic contact layer being selected from the group consisting of: opaque, transparent, and semi-transparent.

16. A method as claimed in claim 15, wherein the second ohmic contact layer is one of blank and patterned.

17. A method as claimed in claim 15 or claim 16, wherein bonding pads are formed on the second ohmic contact layer.

18. A method as claimed in any one of claims 1 to 14, wherein after step (c) ohmic contact formation and subsequent process steps are carried out, the subsequent process steps including deposition of wire bond pads.

19. A method as claimed in claim 18, wherein the exposed second surface is cleaned and etched before the ohmic contact layer is deposited.

20. A method as claimed in any one of claims 15 to 19, wherein the second ohmic contact layer does not cover the whole area of the second surface.

21. A method as claimed in any one of claims 15 to 20, wherein after forming the second ohmic contact layer there is included testing of the semiconductor devices on the epitaxial layers.

22. A method as claimed in any one of claims 15 to 21, wherein there is included the step of separating the layers into individual devices.

23. A method as claimed in any one of claims 1 to 22, wherein the semiconductor devices are fabricated without one or more selected from the group consisting of: lapping, polishing and dicing.

24. A method as claimed in any one of claims 1 to 23, wherein the semiconductor device comprises a plurality of epitaxial layers, a first ohmic contact layer being on a first surface of the epitaxial layers remote from the substrate; the first ohmic contact layers being on p-type layers of the epitaxial layers.

25. A method as claimed in any claim 22, wherein the second ohmic contact layer is formed on n-type layers of the expitaxial layers.

26. A method as claimed in any one of claims 1 to 14, wherein after step (c), dielectric films are deposited on the epitaxial layers and openings are cut in the dielectric films and second ohmic contact layer and bond pads deposited on the epitaxial layers.

27. A method as claimed in any one of claims 1 to 14, wherein after step (c), electroplating of a thermally conductive metal on the semiconductor device is performed.

28. A method as claimed in any one of claims 24 to 26 and claim 27 when appended to any one of claims 24 to 26, wherein the thermally conductive metal comprises copper and the epitaxial layers comprise multiple GaN-related layers.

29. A semiconductor device comprising epitaxial layers, first ohmic contact layers on a first surface of the epitaxial layers, a relatively thick layer of a thermally conductive metal on the first ohmic contact layer to form a heat sink, and a second ohmic contact layer on a second surface of the epitaxial layers an adhesive layer on the first ohmic contact layer between the first ohmic contact layer and the relatively thick layer; the relatively thick layer being applied by electroplating.

30. A semiconductor device as claimed in claim 29, wherein there is a seed layer of the thermally conductive metal, applied to the adhesive layer.

31. A semiconductor device as claimed in any one of claims 29 and 30, wherein the relatively thick layer is at least 50 micrometers thick.

32. A semiconductor device as claimed in any one of claims 29 to 31, wherein the second ohmic contact layer is a thin layer in the range of from 3 to 500 nanometers.

33. A semiconductor device as claimed in any one of claims 29 to 32, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

34. A semiconductor device as claimed in any one of claims 29 to 33, wherein the second ohmic layer includes bonding pads.

35. A semiconductor device as claimed in any one of claims 29 to 34, wherein the thermally conductive metal is copper and the epitaxial layers comprise multiple GaN-related epitaxial layers.

36. A semiconductor device as claimed in any one of claims 29 to 35, wherein the semiconductor device is selected from the group consisting of: a light emitting device, and a transistor device.

37. A semiconductor device comprising epitaxial layers, a first ohmic contact layer on a first surface of the epitaxial layers, an adhesive layer on the first ohmic contact layer, and a seed layer of a thermally conductive metal on the adhesive layer.

38. A semiconductor device as claimed in claim 37, further including a relatively thick layer of the thermally conductive metal on the seed layer, the relatively thick layer acting as a heat sink.

39. A semiconductor device as claimed in claim 37 or claim 38, further including a second ohmic contact layer on a second surface of the epitaxial layers; the second ohmic contact layer being a thin layer in the range of from 3 to 500 nanometers.

40. A semiconductor device as claimed in any one of claims 37 to 39, wherein the second ohmic contact layer comprises bonding pads and is selected from the group consisting of : opaque, transparent, and semi-transparent.

41. A semiconductor device as claimed in any one of claims 37 to 40, wherein the thermally conductive metal comprises copper; and the epitaxial layers comprise GaN-related layers.

42. A method of fabrication of a semiconductor device, the method including the steps:
(a) on a substrate with a plurality of epitaxial layers comprising multiple GaN-related epitaxial layers, forming a first ohmic contact layer on a first surface of the epitaxial layers;
(b) removing the substrate from the epitaxial layers; and
(c) forming a second ohmic contact layer on a second surface of the epitaxial layers, the second ohmic contact layer having bonding pads formed thereon.

43. A method as claimed in claim 42, wherein the second ohmic contact layer is selected from the group consisting of: opaque, transparent, and semi-transparent.

44. A method as claimed in claim 42 or claim 43, wherein the second ohmic contact layer is one of: blank, and patterned.

45. A semiconductor device fabricated by the method of any one of claims 42 to 44.

46. A semiconductor device as claimed in claim 45, wherein the semiconductor device is one of: a light emitting device, and a transistor device.

47. A method for fabrication of a semiconductor device on a substrate, the semiconductor device having a plurality of layers with a device layer; the method including the steps:
(a) electroplating a layer of a thermally conductive material onto a surface of the semiconductor device remote from the substrate and close to the device layer; and
(b) removing the substrate.

48. A method as claimed in claim 47, wherein the semiconductor device is a silicon-based device.

49. A method for fabrication of a light emitting device on a substrate, the light emitting device having a plurality of layers with an active layer; the method including the steps:

(a) electroplating a layer of a thermally conductive material onto a surface of the semiconductor device remote from the substrate and close to the active layer; and

(b) removing the substrate.

50. A method as claimed in any one of claims 47 to 49, wherein the thermally conductive layer is as a heat sink.

51. A method as claimed in claim 50, wherein the thermally conductive layer is of a thickness in the range of from 3 microns to 300 microns.

52. A method as claimed in claim 50 or claim 51, wherein the thermally conductive layer is of a thickness of from 50 to 200 microns.